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RESEARCH ARTICLE

Design Ratio-Memory Cellular Neural Network (RMCNN) in CMOS Circuit Used in Association-Memory Applications for 0.25 mm Silicon Technology

Jui-Lin Lai[1,*] and Chung-Yu Wu[2]

[1]*Department of Electronic Engineering, National United University, MiaoLi City 36003, Taiwan*
[2]*Department of Electronic Engineering, National Chiao-Tung University, Hsinchu 300, Taiwan*

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Abstract: The paper is proposed the Ratio-Memory Cellular Neural Network (RMCNN) that structure with the self-feedback and the modified Hebbian learning algorithm. The learnable RMCNN architecture was designed and realized in CMOS technology for associative memory neural network applications. The exemplar patterns can be learned and correctly recognized the output patterns for the proposed system. Only self-output pixel value in A template and B template weights are updated by the nearest neighboring five elements for all test input exemplar patterns. The learned ratio weights of the B template are generated that the catch weights are performed the summation of absolute coefficients operation to enhance the feature of recognized pattern. Simulation results express that the system can be learned some exemplar patterns with noise and recognized the correctly pattern. The 9×9 RMCNN structure with self-feedback and the modified Hebbian learning algorithm is implemented and verified in the CMOS circuits for TSMC 0.25 μm 1P5M VLSI technology. The proposed RMCNN have more learning and recognition capability for the variant exemplar patterns in the auto-associative memory neural system applications.

Keywords: Auto-Associative Memory, Cellular Neural Network (CNN), Ratio-Memory (RM), Template.

INTRODUCTION

The Cellular Neural Network (CNN) has properties for the neighboring cells with locally connected as introduced by Chua and Yang [1, 2]. Among from the more learning methods was published in the literature. The coefficients of template in the CNN are found by the perception-learning rule. The network can be easily implemented in VLSI for various image operations. Thus, the CNN with the specific template in the image processing have been mentioned [3 - 7]. It can learn the exemplar patterns and recognize correctly pattern output.

The most designed neural networks were stored the processed patterns has a local minimum of an associative energy function in the associative memory. Associative memory research is an important application in the neural network. The CNN has been integrated learning algorithm to generate associative memories used by the dynamic equation learn algorithm for the image patterns learn and recognition [6 - 10].

The modified Hopfield network and the discrete Hebbian learning are applied in the neurons of CNN. The Grossberg outstar structure is consisted the ratio memory (RM) to implement the weights of template use in the neural network for various image processing. The weights of the **A** template is accumulated from the selected cell and it's the nearest neighboring four cells for the exemplar input patternthat the processed **A** template is produced by ratio-memory. The structure with associative-memory can be realized that the neural system with 9x9(18x18) array through learn can recognize 3 (5) patterns with Gaussian noise. The 18x18 RMCNN is included coupled **A** template and the self-feedback

* Address correspondence to this author at the Department of Electronic Engineering, National United University, MiaoLi City 36003, Taiwan; Tel: +886-37-382510; Fax: +886-37-382498; E-mail: jllai@nuu.edu.tw

from output be able to learn and recognize 87 noisy patterns with noise at variance 0.3 [15 - 19].

The capability and function of the 18×18 RMCNN architecture with coupled the embedded ratio-memory **B** template and the modified Hebbian learning algorithm is shown and analysed. The structure of the RMCNN with **B** template and the modified Hebbian learning algorithm are fabricated in the VLSI circuits for the TSMC 0.25 μm 1P5M CMOS technology. The system has ability to learn 8 patterns with white-black noise and successfully recognized. The capability of pattern learning and recognition is improved for the proposed system.

The CNN with reconfigurable was developed to meet the various applications [20 - 23]. To design the distinct new synaptic weighting circuit is provided for the pattern recognition, medical detection process and special applications [24 - 29].

The paper arranged as follows. First part presented the RMCNN structure with the modified Hebbian learning and the embedded ratio-memory. The second part, the VLSI structure and its CMOS circuit realization are described. In third part, the analyses of RMCNN and simulation results demonstrate for patterns learning and recognition. Finally, the conclusions are given.

RMCNN ARCHITECTURE

Cellular Neural Network with parallel processing function can expanded in the massive scale to suit the neuron morphic applications. In a two-dimensional CNN, each cell is just only connected to its neighboring cells, the weights expressed the connected line segment, $X_{ij}(t)$ is the state and $Y_{ij}(t)$ is the output of a regular cell which can be expressed by mathematic model as equations (1) and (2) [1, 2].

$$\dot{\mathrm{X}}_{ij}(t) = -\mathrm{X}_{ij}(t) + \sum_{C(k,l)\in Nr(i,j)} a_{ijkl}(t)\mathrm{Y}_{kl}(t) + \sum_{C(k,l)\in Nr(i,j)} b_{ijkl}(t)u_{kl} + \mathrm{z}_{ij} \tag{1}$$

$$y_{ij} = f(x_{ij}) = \frac{1}{2}\left|x_{ij}+1\right| - \frac{1}{2}\left|x_{ij}-1\right| \tag{2}$$

where $Y_{kl}(t)$ is output and U_{kl} is input of the cell C(k, l) in the r-neighborhood system ($Nr(i, j)$), z_{ij} is threshold value of the cell C(i, j), f is bipolar activation function, and $\mathrm{a_{ijkl}}$ and $\mathrm{b_{ijkl}}$ are expressed the weights from $Y_{kl}(t)$ and U_{kl} for the cell C(i, j), respectively.

In the paper, the proposed CNN structure consisted of the uncoupled **A** template and coupled **B** template with r=1 neighborhood. The coefficient of the space-variant **B** template corresponds to the input and the nearest four neighboring inputs of the cell C(i,j). The fixed (Dirichlet) boundary condition is commonly used in the outermost boundary cells. Those edge cells are preset to zeros. The **A** template just only takes one self-feedback coefficient. The **A** and **B** templates are expressed as

$$A_{ij}^{1} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 0 \end{bmatrix} \quad \boldsymbol{B}_{ij}^{1} = \begin{bmatrix} 0 & b_{ij(i-1)j} & 0 \\ b_{iji(j-1)} & b_{ijij} & b_{iji(j+1)} \\ 0 & b_{ij(i+1)j} & 0 \end{bmatrix} \tag{3}$$

A CNN include the ratio-memory (RM) that the expressed RM and SRM blocks are used to realize the weights connect from the neighboring cells and the self-cell, respectively, is shown in Fig. (**1a**). The learned weights are transformed into the ratio weight $\mathrm{wb_{ijkl}}$ arestored the associative memory in the ratio-memory (RM) model at an equilibrium state as

$$\mathrm{x}_{ij}(k+1) = \sum_{C(k,l)\in N_r(i,j)} wb_{ijkl}(k)\cdot \mathrm{u}_{kl}(k) + y_{ij} + \mathrm{z}_{ij} \tag{4}$$

The equilibrium state X is globally asymptotical stable based on the locally stable by the energy function and the globally attractive for the CNN behavior model. The RMCNN is realized to store a large set of exemplar patterns for the recurrent auto-associative memory [11 - 17]. The RMCNN is training through the input test exemplar patterns to update the weights of the **B** templates and output the desired pattern. The obtained output pattern is according to the

information between input pattern and weight matrix.

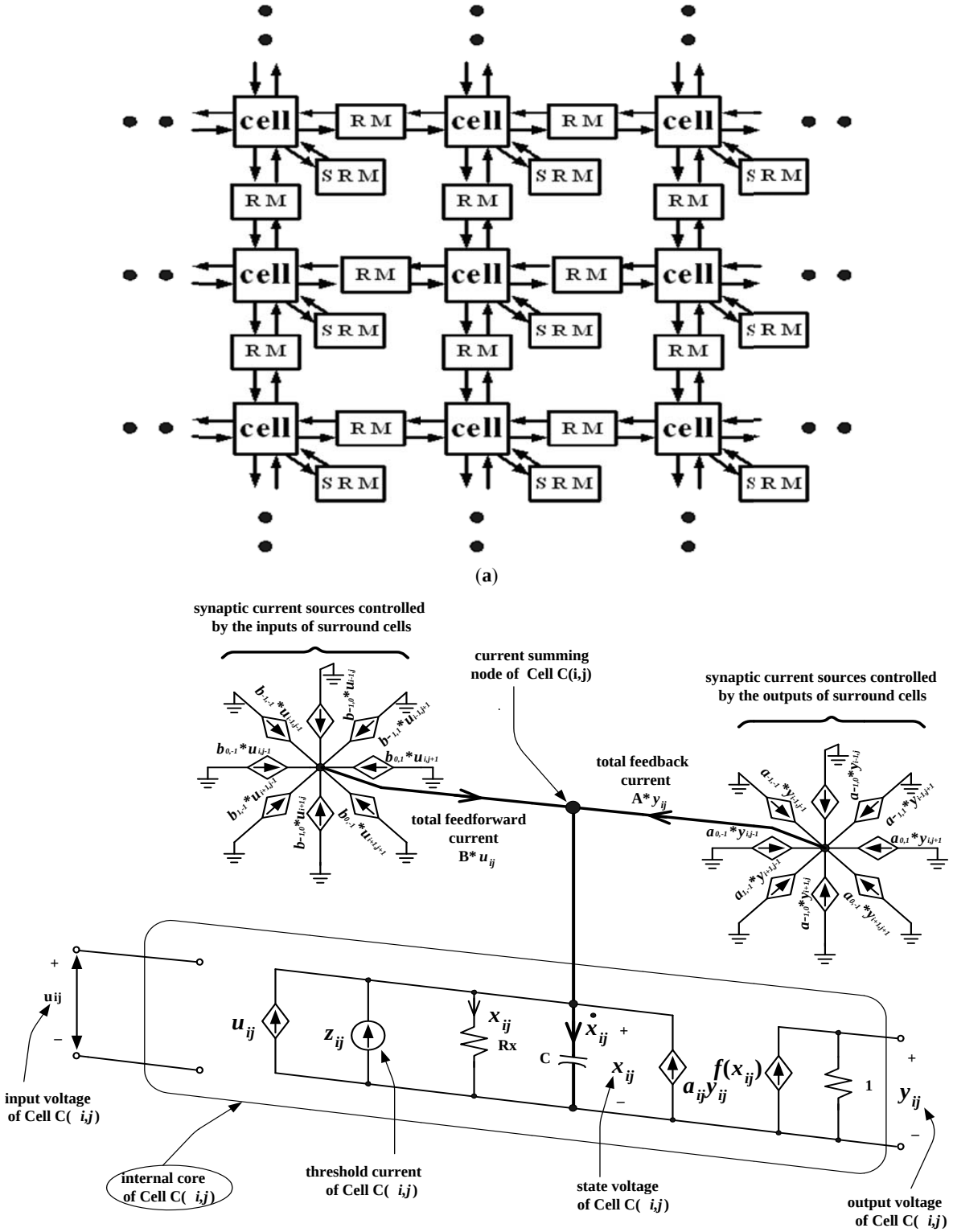


Fig. (1). (**a**) CNN with RM structure, (**b**) C(*i*, *j*) cell realization [4].

The variables u_{ij}, x_{ij}, and y_{ij} of CNNs are expressed to voltages and z_{ij} is a bias current in the VLSI implementation. The block diagram of a cell is realized by electronic circuits, as shown in (Fig. **1b**). The signal flow structure of a cell

C(i,j) can be expanded to the standard CNN {**A**, **B**, **Z**} with a single neighborhood cell. The arrows indicate the parallel data paths from the input u_{kl} and the output y_{kl} of the neighboring cells *C(k,l)*, respectively. The thinness line on arrows denotes the threshold z_{ij}, input u_{ij}, state x_{ij}, and output y_{ij}, respectively.

In the learned period, the weight-learning algorithm integrated with the modified Hebbian learning algorithm is applied to find the increment dw_{ij} of the weight vector in the learning block, is shown in (Fig. **2**). The recursive update operation was generated for m distinct patterns at time t=0 as

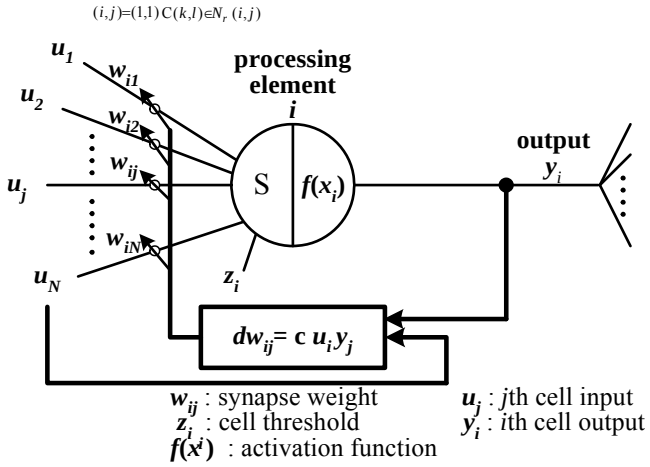


Fig. (2). Illustration for weights learning algorithm.

$$Wb_{ijkl}(0) = \sum_{p=1}^{m} y_{ij}^{p} u_{kl}^{p} \qquad C(k,l) \in N_r(i,j) \tag{5}$$

$$br_{ijkl}(0) = \frac{wb_{ijkl}(0)}{\sum_{C(k,l)\in N_r(i,j)} \left| wb_{ijkl}(0) \right|} \tag{6}$$

The weights of **B** template updated the values in parallel and the operation is ended until all patterns are learned during the learning period. The weights $Wb_{ijkl}(0)$ can be normalized to bounded the weight value. The normalized weights $br_{ijkl}(0)$ are stored in the ratio-memory.

In the elapsed period, the voltage on the stored capacitor C_{zs} is gradually decreased by $I_{leakage}$ of the leakage current. Assume the leakage current is nearly constant leakiness so the stored voltage on capacitor $C_{zs}$is decreased by the function of time, as

$$\left| br_{ijkl}(t) \right| = \left| br_{ijkl}(0) \right| - \frac{I_{leakage}}{Czs}\ t \tag{7}$$

In the recognition period, the system is used RM to normalize the coefficientsof **B** template. The operation of normalization is active like as the spatial averaging. The normalized operation of patterns depended on spatial operations for the local neighborhoods of the cell inputs are performed. Using ratio-memory approach to transform the normalized weights $br_{ijkl}(t)$ into the ratio weight b_{ijkl} of **B** template as [15].

$$b_{ijkl}(t) = \frac{br_{ijkl}(t)}{\sum_{C(k,l)\in N_r(i,j)} \left| br_{ijkl}(t) \right|} \tag{8}$$

The ratio weight $b_{ijkl}(t)$ is generated by the M/D block to produce the normalized effect and enhance the feature of the pattern. When the larger intensity of the weight b_{ijkl} of cell C(*i*,*j*), the weight is gradually increased. Otherwise, the

weight gradually decreased. As the simulation results show that the ability of the RMCNN with the ratio-memory was improved for the noisy patterns recognition.

In the recognition state, the cell outputs are adjusted by the learned ratio weights gradually to close one of the features for the training patterns. The energy function of a CNN can be expressed in quadratic form as

$$E = -\frac{1}{2}\sum_{ij}\sum_{kl}(b_{ijkl}u_{kl})Y_{ij} \quad \mathbf{(9)}$$

The energy function is also tendency converged into the local minimum until all outputs are no more changed. The final recognized pattern is found at the minima of E in the stable state. In (8), the absolute value is added in the denominator because the connection weight br_{ijkl} can be both positive and negative value and the ratio-memory take the total magnitude of each weight element in the ratio-memory to normalize the weight. The stability of the proposed RMCNN needs to further consider an energy function

$$E_{RM} = -\sum_{(i,j)=(1,1)}^{(n,n)}\sum_{C(k,l)\in N_r^0(i,j)} b_{ijkl}u_{kl}y_{ij} \quad \mathbf{(10)}$$

Suppose y_{ij} is changed, then the change of energy can be expressed as

$$\Delta E_{RM} = -\sum_{C(k,l)\in N_r^0(i,j)} b_{ijkl}u_{kl}\Delta y_{ij} - \sum_{(i,j)=(1,1)}^{(n,n)} b_{ijkl}u_{ij}\Delta y_{kl} = \Delta E_{RM1} + \Delta E_{RM2} \quad \mathbf{(11)}$$

The first term ΔE_{RM1} of (11) can be proven to be always non-positive as the proof method in the original Hopfield energy function *E*.

if $\Delta y_{ij} \geq 0$, then $\sum_{C(k,l)\in N_r^0(i,j)} b_{ijkl}u_{kl} \geq 0$

if $\Delta y_{ij} \leq 0$, then $\sum_{C(k,l)\in N_r^0(i,j)} b_{ijkl}u_{kl} \leq 0$

Consider the second energy change term ΔE_{RM2}

$$\Delta E_{RM2} = -\sum_{(i,j)=(1,1)}^{(n,n)} b_{ijkl}\ u_{ij}\ \Delta y_{kl} = -\sum_{(i,j)=(1,1)}^{(n,n)} \frac{br_{ijkl}}{\sum_{C(k,l)\in N_r^0(i,j)} \left|br_{ijkl}\right|}\ u_{ij}\ \Delta y_{kl} \quad \mathbf{(12)}$$

Because the connection weight in the original Hopfield model is symmetric, *i.e.* $w_{ijkl}=w_{klij}$, (12) can be written as

$$\Delta E_{RM2} = -\frac{\sum_{i,j=(1,1)}^{(n,n)} br_{klij}u_{ij}}{\sum_{C(k,l)\in N_r^0(i,j)} \left|br_{ijkl}\right|}\Delta y_{kl} \quad \mathbf{(13)}$$

From equation (13), it can also be proven that ΔE_{RM2} is always non-positive. Thus, under the assumption that the connection weight is symmetric in the original Hopfield model, the stable state of the RMCNN model is also existed.

CMOS CIRCUIT REALIZATION

The function block is proposed to implement the relation operation for the equations (1-8). Taking two neighboring cells *C(i,j)*, *C(k,l)*and their RM block in the RMCNN that the detailed block diagram is shown in Fig. (**3**). The neuron cell is able to summation the current signals from its neighboring cells and self-cell, the stored neuron signal also out to those cells, as Fig. (**1a**). The structure of neuron cell is construct three units for the equivalent R_{ij} and C_{ij} storage element, V-I converter (T1), and V-I converter with sign-detect (T2D). The transmitted signals need the ratioed weight is calculated by the RM model. The RM block is consisting of the M/D and S block that the current mode circuit of

M/D block is combined four-quadrant multiplier and two-quadrant divider [13 - 17]. The ratio weight is generated by the distinct product for the neighboring weights in the **B** template that the result of the product term for the learned weight base on the equation (5) in the learning period.

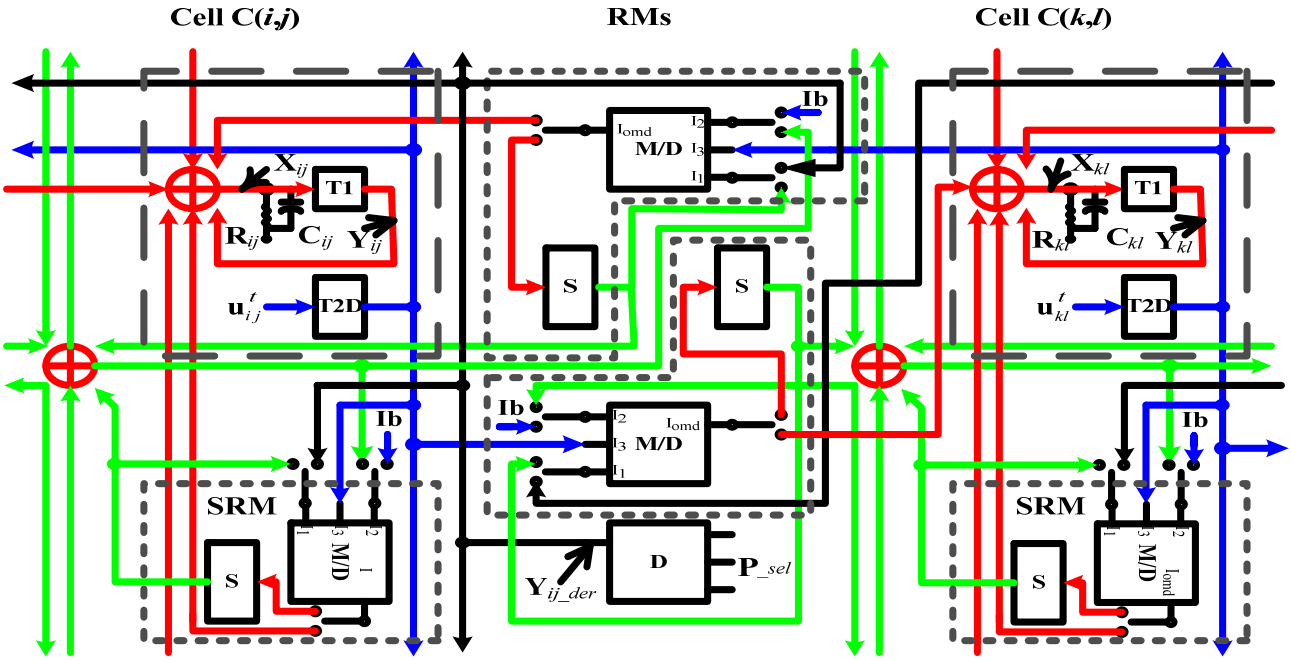


Fig. (3). The architecture of two neighboring cells and ratio memory (RM) in the RMCNN.

The storage block (S) described in the detailed block diagram is shown in Fig. (**4**). Fig. (**4a**, **4b**) are expressed the learning and the recognition operations for the associative memory, respectively. T2L block is used to store the absolute voltage value from C*zi* to C*zs* and the latch circuit stored its sign signal. The resistor R*zs* in parallel with C*zs* is induced the inevitable RC time constant leakage. The V-I converter is provided by T3 block to convert the voltage value stored in C*zs* into current flow. The capacitor C*zi* use to store the weight $zi_{ijkl}$with absolute resultant during the learning period.

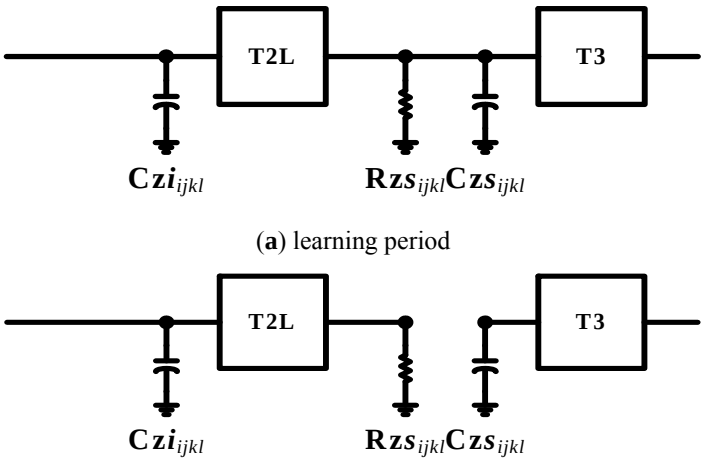


Fig. (4). Learning and recognition operation in the S block of RMCNN.

The Iy^{p}_{ij}(Iu^{p}_{kl} current product directly charging on C*zi* generated the weight voltage Vzi_{ijkl}*(0)* at $t = 0$. When the end of learning period then the voltage can be written as

$$\mathrm{Vzi}_{ijkl}(0)=\frac{1}{\mathrm{Czi}}\sum_{p=1}^{m}\left(\int_{T_P}\frac{\mathrm{Iy}_{ij}^{p}\mathrm{Iu}_{kl}^{p}}{\mathrm{Ib}}dt\right)\qquad C(k,l)\in N_r(i,j) \tag{14}$$

where Iy^{p}_{ij} is a current of the pixel of the *p*-th desired patterns at *i*-th row and *j*-th column, Iu^{p}_{kl} is a current for the pattern input to the cell C(*k*, *l*) at *Nr*(*i*, *j*) neighboring cells, Ib is setting a constant bias current, $\mathrm{Vzi}_{ijkl}(0)$ is stored on C*zi* voltage of the weight W_{ijkl} at $t = 0$ sec, and T_P is the learning time for each the learned patterns.

In the M/D block, the four-quadrant multiplier and the two-quadrant divider is used to generate the ratioed weight. The product current for the five ratioed weights to the neighboring five input cells current signal was summed during the recognition period. The voltage of cell state $\mathrm{X}_{ij}(t)$ is converted through R_{ij} and C_{ij}. As equation (15) is shown the $\mathrm{Vx}_{ij}(t)$ expression.

$$\mathrm{Vx}_{ij}(t)=\mathrm{R}_{ij}\left(\sum_{\mathrm{C}(k,l)\in N_r^0(i,j)}\frac{\mathrm{Iu}_{\mathrm{kl}}(t)\mathrm{Izs}_{ijkl}(t)}{\sum_{\mathrm{C}(k,l)\in N_r^0(i,j)}abs[\mathrm{Izs}_{ijkl}(t)]}+\mathrm{Iy}_{ij}^{t}\right) \tag{15}$$

The sign of $Vzi_{ijkl}$is detected and latched in the dynamic latch CMOS circuits for the T2L block shown in Fig. (**5**). Integrated the analog multiplier with four-quadrant and the divider with two-quadrant to realize the current mode M/D CMOS circuit shown in Fig. (**6**). The multiplication input currents I_1 and I_3 are provided from the PMOS current mirror M14i/M14 and M14i/M15/M16, respectively, and the divider input current I_2 is through the M24i/M24 pair. The operational amplifier (op-amp) and NMOS device M21 is combined to a closed-loop feedback form. Base on the properties of the operational amplifier to know the voltage of V_{E3} and V_{E4} are virtually identity at the emitter terminal. The PNP bipolar junction transistors (BJTs) Q1, Q2, Q3, and Q4 are adopted to perform the multiplication and division operations depend on the relation between base-emitter voltage V_{BE} and emitter current I_E as

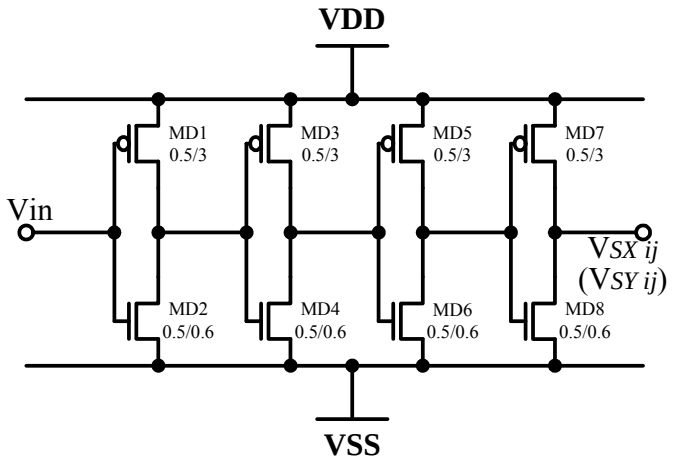


Fig. (5). Sign detector.

$$\mathrm{I}_E=\mathrm{I}_S\exp\left(\mathrm{V}_{BE}/\mathrm{V}_T\right)\quad\text{or}\quad \mathrm{V}_{BE}=\mathrm{V}_T\ln\left(\mathrm{I}_E/\mathrm{I}_S\right) \tag{16}$$

where I_S is the saturation current of PN junction and V_T is the thermal voltage. The load current I_4 is provided through M19, M20, M25, and M26 PMOS current mirrors pairs, and the sink current from the M29 and M30 NMOS current mirror pair to flow the output current I_{omd}.

The op-amp has an identical input property that the loop voltage $\mathrm{V}_{BE1}+\mathrm{V}_{BE3}$ is equal to $\mathrm{V}_{BE2}+\mathrm{V}_{BE4}$. Therefore, among the I_{E1}, I_{E2}, I_{E3}, and I_{E4} can be derived the relationship equation from equation (16) as

$$\mathrm{I}_{E4}=\frac{\mathrm{I}_{E1}\ \mathrm{I}_{E3}}{\mathrm{I}_{E2}} \tag{17}$$

Using XNOR gate to control the flow direction of output current is determined according to the sign of input and weight for the M/D.

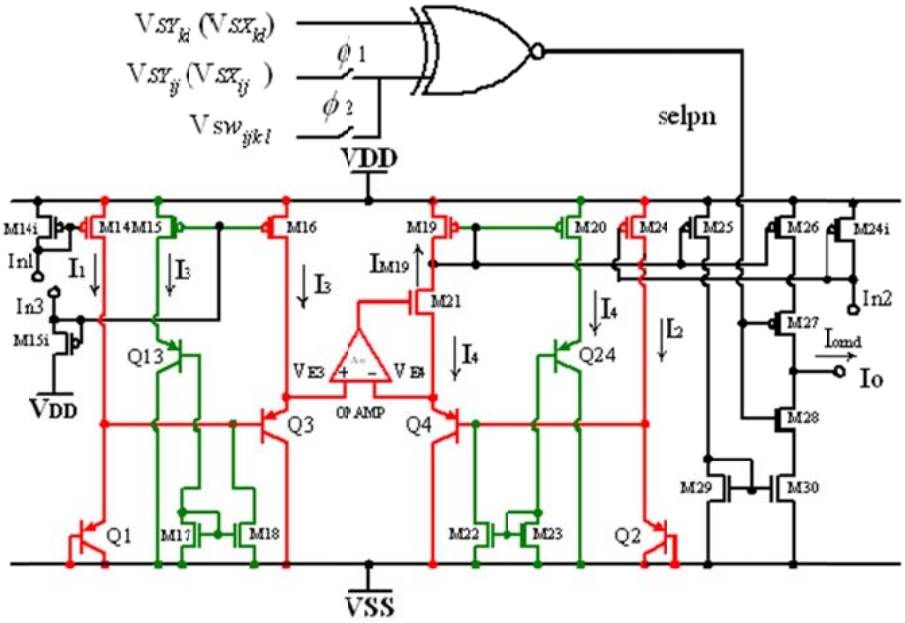


Fig. (6). The CMOS circuit of the M/D block.

The M/D circuit function is simulated through HSPICE shows that the results are correctly verified for the multiplier and divider, are shown in Fig. (**7a**, **b**), respectively. Fig. (**8**) expressed the CMOS circuits of T2, where Fig. (**8a**) show that the absolute-value V-I converter circuit, the output absolute current *vs* the input voltage transfer curve is shown in (Fig. **8b**). The V-I converter is consist of the CMOS differential amplifier M1~M7 that the source resistance to increase the linear range also to realize for T1 and T3 blocks. The absolute-value circuit is loaded the output current *Iovic* by M8~M13 to output the direction of the unified flow from the absolute-value current *Ioabs*.

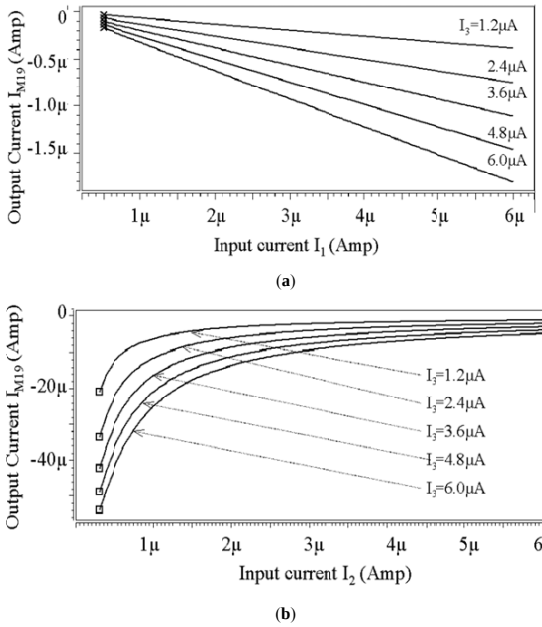
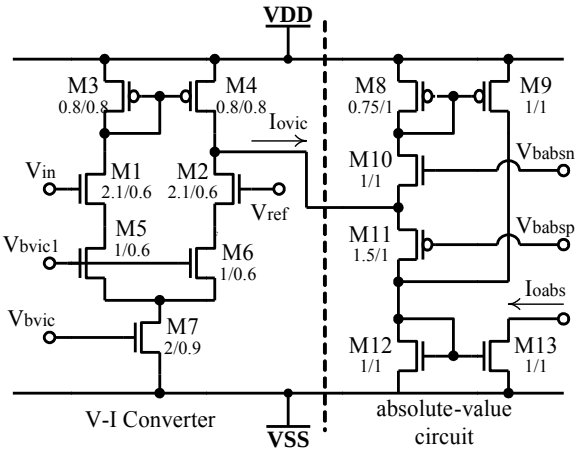
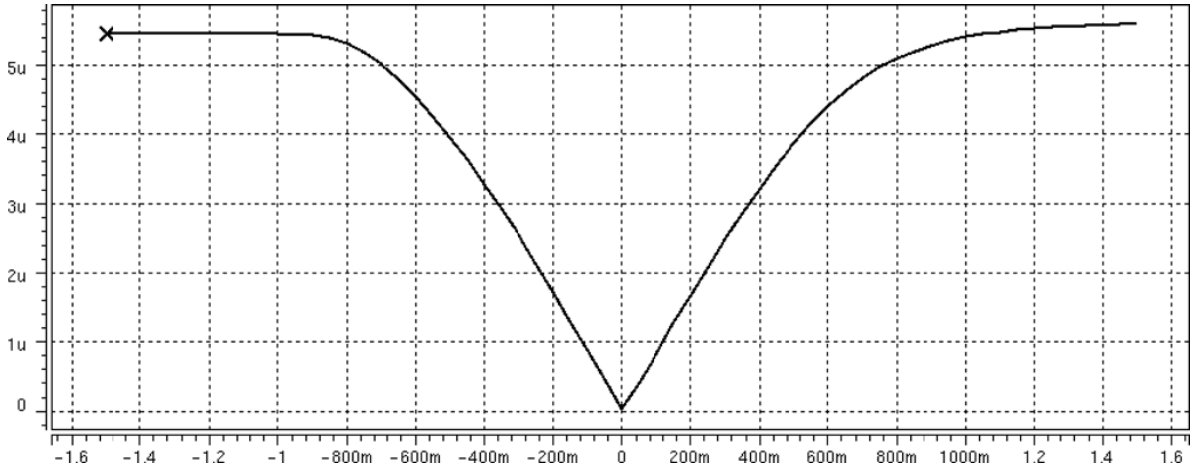


Fig. (7). HSPICE simulation results: (**a**) Multiplication function with I_2=20μA, and (**b**) Division function with I_1=6μA.



(**a**) V-I converter and absolute-value circuit



(**b**) Simulation results

Fig. (8). The circuit of T2 and HSPICE simulation results.

SIMULATION RESULTS

The structure of the proposed 18×18 RMCNN included the coupled **B** template, only self-feedback in **A** template, and the modified Hebbian learning algorithm at the direct neighborhood (r=1) that the associative memory is simulated by Matlab software. The black pixel is settled to +1 and the white pixel to -1 in the processed pattern for the RMCNN. In the system, assume parameters for the constant leakage current 0.8fA and the associative memory storage capacitor Czs of 2pF are used in the simulation. The weights of **B** template are processed into ratio weights to operate each cell in the system for the learning period. The English characters A with white-block noise is adopted the test patterns, is shows in Fig. (**9**). As the simulating results show that the RMCNN with **B** template can be learned eight noisy patterns with white-block noise and successfully recognized those patterns and the correctly output the desired pattern of the character **A**. The function of RMCNN is verified and success rate can reach to 97%.

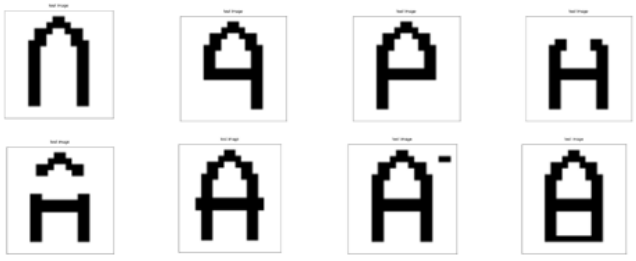


Fig. (9). Test patterns with white-black noise Elapsed time factor.

The required waiting time for the correctly pattern recognition is related to the elapsed time factor from the simulation results. The elapsed time is normalized 50 second to the elapsed time factor. Observe the error function between the desired pattern and the output pattern that the variation of the error is decreased by the function of the elapsed time factor for each exemplar test patterns during the elapsed time. The error is reduced to zero at the elapsed time factor over 9 for the various test patterns, which is 450 second as shown in Fig. (**10**).

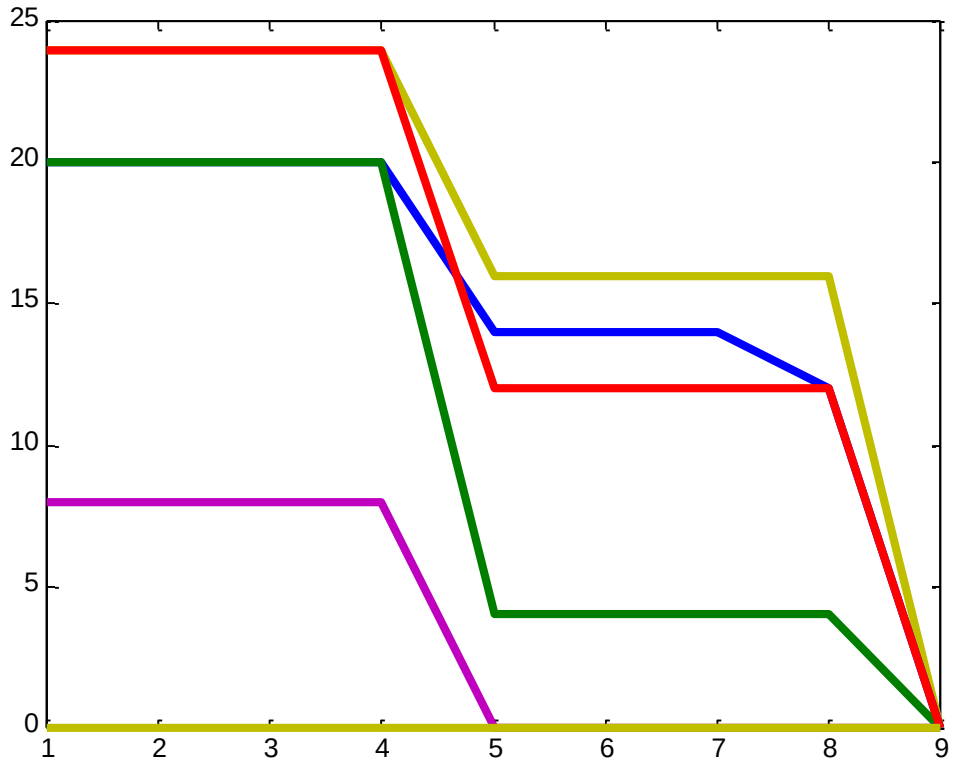


Fig. (10). Error functions during elapsed time factor.

The exemplar patterns are presented the normal, expand, left-rotate, right-rotate, and reversal of the A character, as shown in Fig. (**11**). The desired RMCNN outputs are the pattern A. While the test pattern of the expanded A character into the RMCNN as the first one shown in the Fig. (**12**). The processing procedure of the recognition is presented from the 2nd to 8th patterns, the last one is the final recognized correctly output pattern. Another test case, using the left-rotate A character in the RMCNN to process the image recognition. In the Fig. (**13**) show that the resultant of the recognition in sample for the 150 times iterations and the correct pattern at the last one in the figure is recognized. Thus, the RMCNN with **A** and **B** template can be recognized by the learned ratio weights for the complex test example pattern.

Fig. (11). Test patterns of character A with normal, expanded, left-rotate, right-rotate, and reversal types.

Fig. (12). Recognition sequence of expanded A character during recognition period.

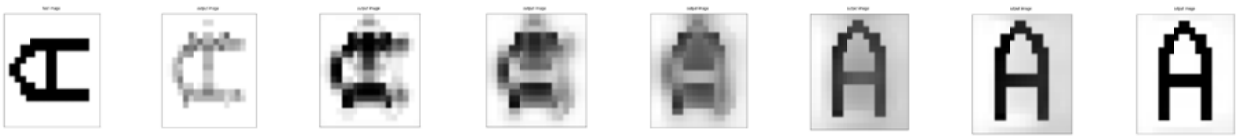
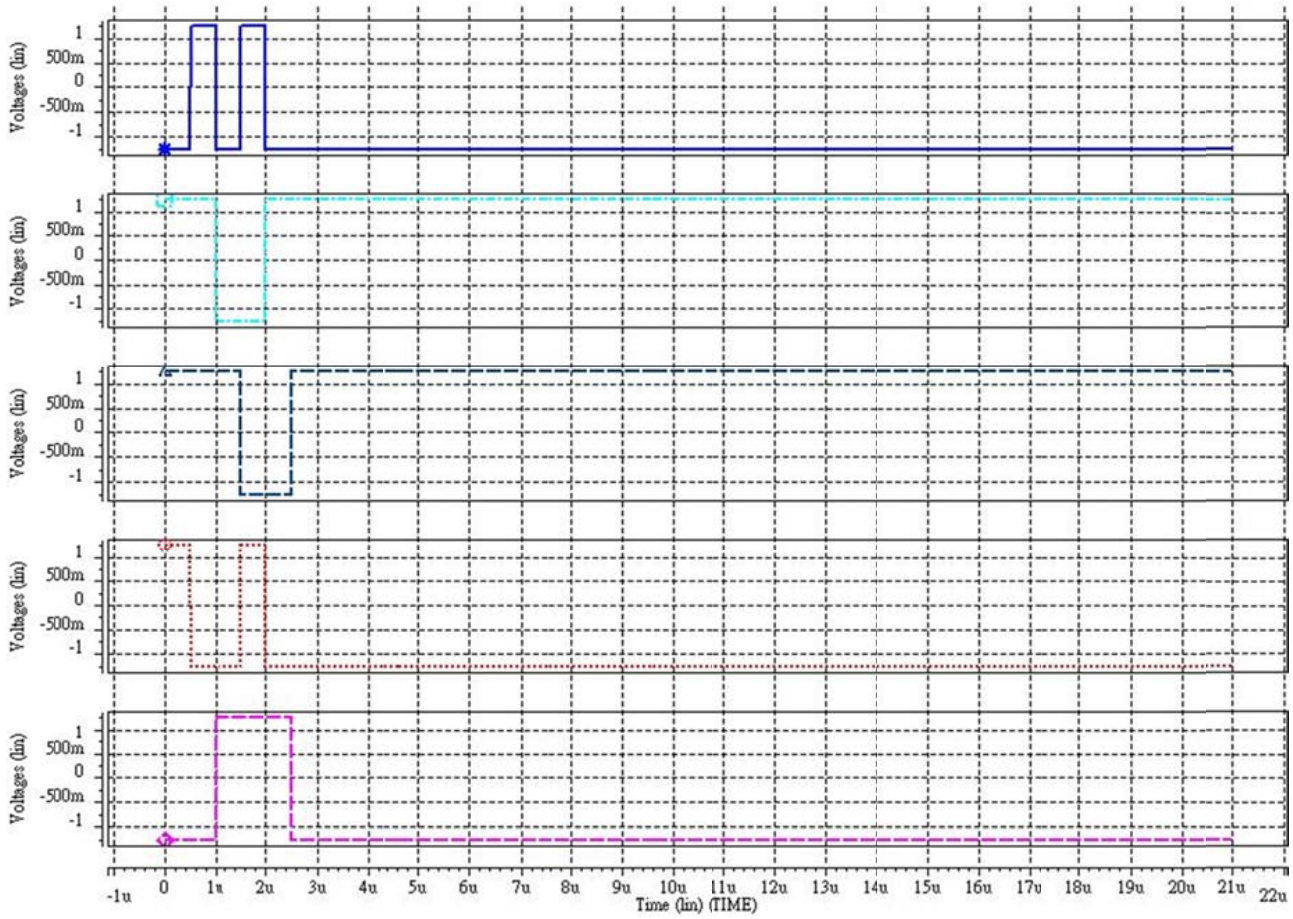


Fig. (13). Recognition sequence of left-rotate A character during recognition period.

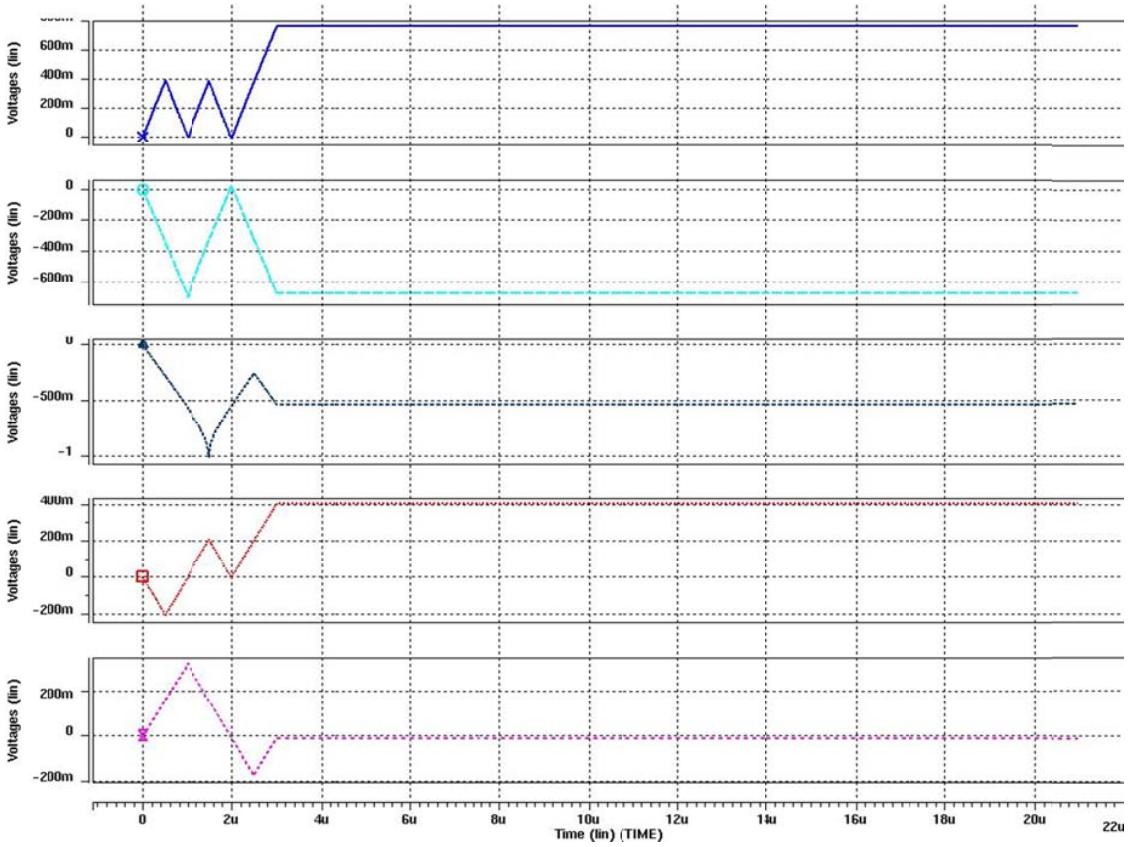
The capability of the pattern recognition has been verified for the proposed 18x18 RMCNN with **B** template. The function blocks of the architecture are completely designed in the CMOS circuits and also integrated in VLSI technology.

The approach of the ratio-memory used to provide the function for feature enhancement in the image processing. The effect of the ratioed weight is shown that the larger weights are gradually increased to 1 with time. Otherwise, the smaller weights are gradually decreased to zero. The five weights are learned and ratioed for the time of learned and the elapsed period that the variations of the ratioed weights are shown in Fig. (**14**).

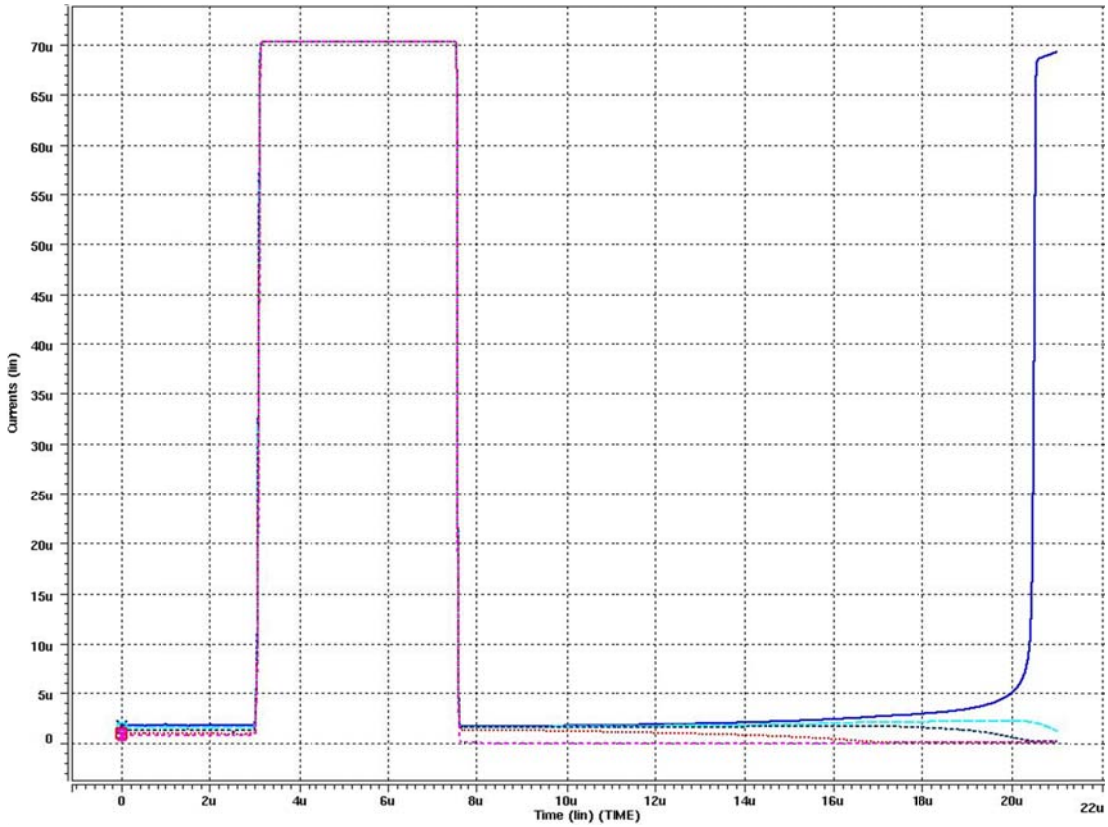
The structure of the proposed 18x18 RMCNN with **B** template is implemented and simulated in CMOS circuit by the HSPICE. The weights of the **B** template is sequentially updated for five exemplar patterns per each charge time with the period 0.5μs are applied and the ratioed-memory are used to store the ratioed weights. The incompletely English character H of the exemplar pattern is shown in the left of Fig. (**15**). Simulation results show that the RMCNN be able to recognize the correctly output pattern for the test input exemplar pattern, as shown in the right of Fig. (**15**). The system has capability to learning exemplar pattern and recognizing the correct pattern for the image process applications.



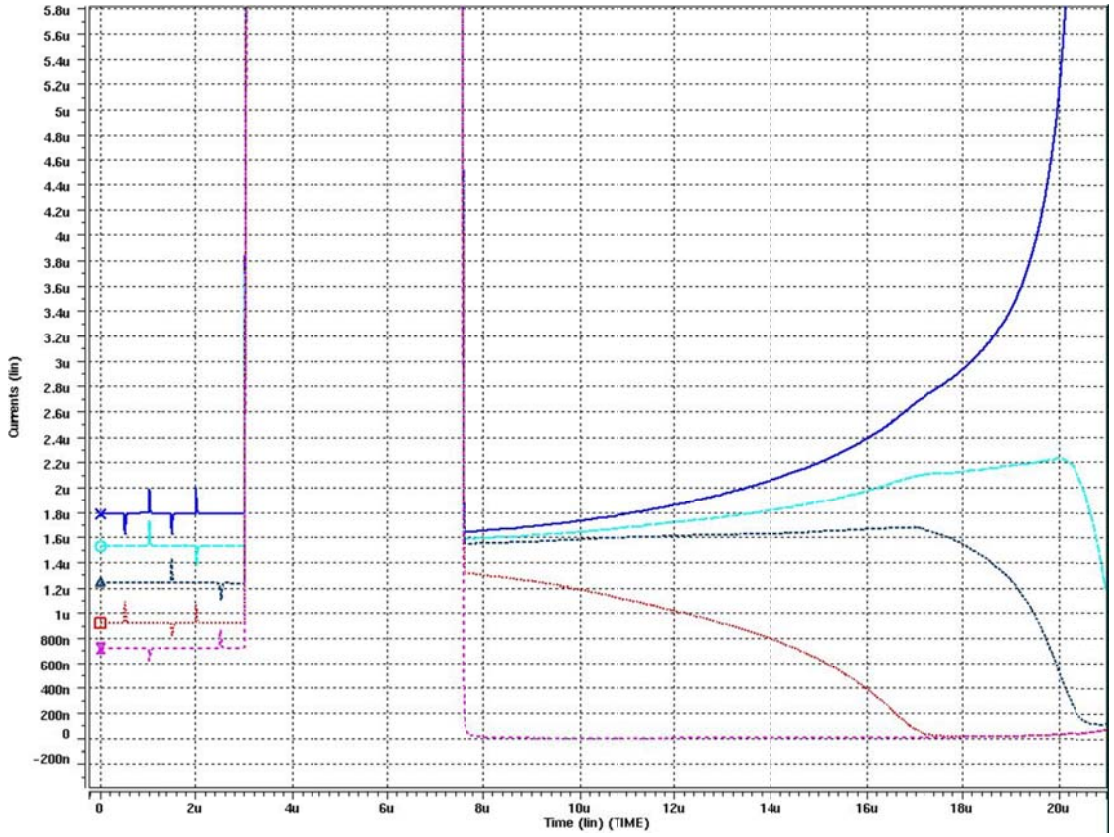
(**a**)


Voltages (lin)
600m
400m
200m
0
Voltages (lin)
0
-200m
-400m
-600m
Voltages (lin)
0
-500m
-1
Voltages (lin)
400m
200m
0
-200m
Voltages (lin)
200m
0
-200m
0
2u
4u
6u
8u
10u
12u
14u
16u
18u
20u
22u
Time (lin) (TIME)

(**b**)


Currents (lin)
70u
65u
60u
55u
50u
45u
40u
35u
30u
25u
20u
15u
10u
5u
0
0
2u
4u
6u
8u
10u
12u
14u
16u
18u
20u
22u
Time (lin) (TIME)

(**c**)



(**d**)

Fig. (14). RMCNN (**a**) learn data with the five neighboring cells for six data input; (**b**) the learned weights; (**c**) learning and ratio state; (**d**) the ratioed weights during the elapse time.

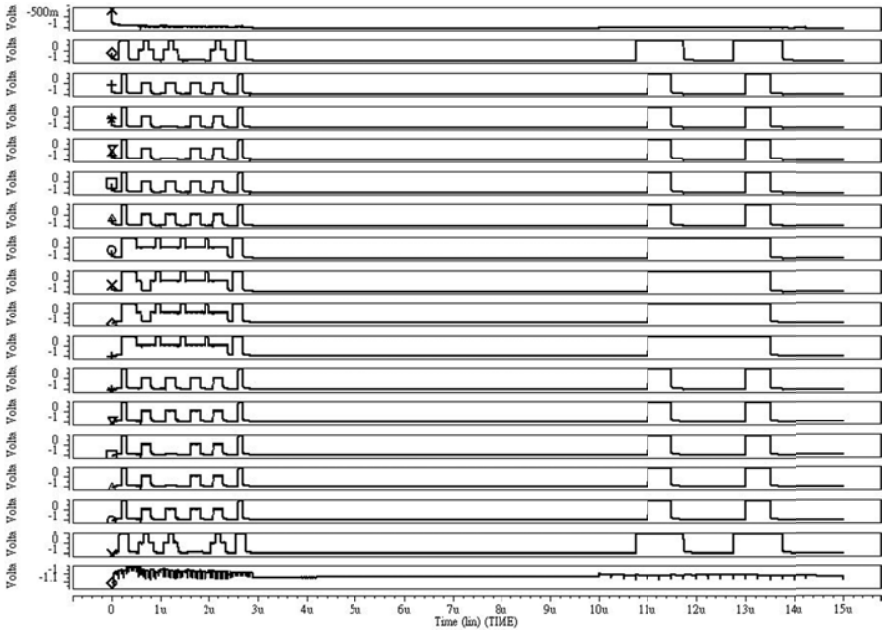


Fig. (15). The recognized pattern for 18 x 18 RMCNN.

The chip of 9x9 RMCNN is designed with the learning and recognition operations by the TSMC 0.25μm 1P5M technology that the layout graph is shown in Fig. (**16**). The layout chip of 9x9 RMCNN includes 81 regular cells, 405

RMs and 81 current summations in wafer area 4000μm x 4200μm is implemented and verified. As simulation results successful verified the 18x18 RMCNN also have the correct function for patterns recognition. The combination of four chips is constructed the 18x18 RMCNN structure to use for auto-associative memory applications.

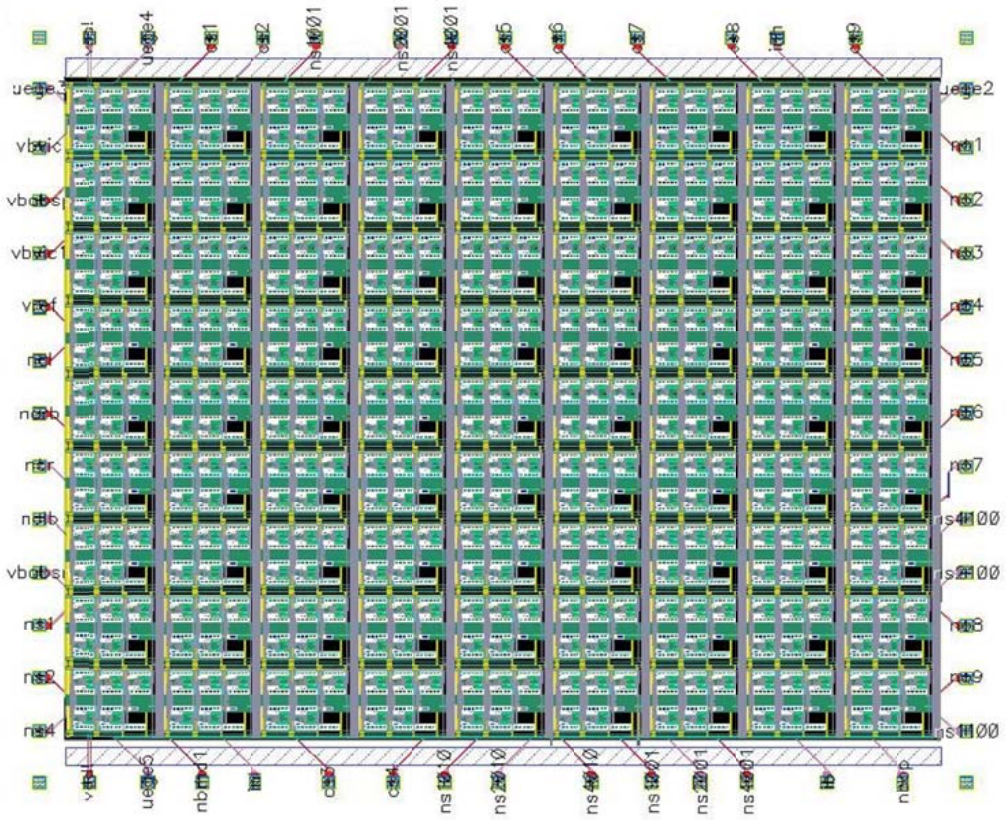


Fig. (16). Layout graph for 9x9 RMCNN chip.

CONCLUSION

The paper is proposed and analyzed the ratio-memory cellular neural networks (RMCNN) with **B** template and self-feedback for pattern recognition in the associative memory. The five weightsin the **B** template of RMCNN can generated and updated from the exemplar patterns that the weights are ratioed from the absolute summation for the neighborhood cells and stored the weights in the ratioed-memory. To observe the simulation results, the function of 18×18 RMCNN has been verified that system can learned 8 patterns with white-black noise of the character A and correctly recognized the desired pattern. The more than one-desired English characters are learned to reduce the recognition rate. The proposed RMCNN can provided the more ability for learn and recognition than the CNN without RM and its complexity is less than the Hopfield neural network. Moreover, the capability of the pattern learning and recognition for the proposed RMCNN with the modified Hebbian learning algorithm is improved. The architecture of RMCNN is successfully implemented by TSMC 0.25μm 1P5M CMOS silicon technology in VLSI structure. The learnable 9x9 RMCNN VLSI chip can expend into the 18x18 neural networks system to develop more complexity bio-image processing for real-time applications.

CONFLICT OF INTEREST

The authors confirm that this article content has no conflict of interest.

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DISCLOSURE

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