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RESEARCH ARTICLE

To Design a Cascode LNA by Using Channel-Length-Split Device with Constant-g$_m$ in a 0.35 µm Silicon CMOS Technology

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Abstract: In the paper, the folded-cascode low-noise operational amplifier (LNA) with constant-gm is proposed and analyzed. The channel-length split technique adopted to expand ratio of W/L of the differential pair transistor to improve the performance of LNA for the gain bandwidth product, noise and offset voltage. The channel-length split method is separated differential input transistor into 2 transistors in series. The area of the transistor (W, L) can be properly increased to effectively decrease the flick noise. The double indirect-frequency compensation technique and the clamping circuit are adopted in amplifier to increase the bandwidth. The proposed two sets input differential pair can be provided a constant-gm value and rail-to-rail swing during the operating region. The floating-point structure is used to reach rail-to-rail swing at output stage. Simulation results show that the gain, constant-gm in input stag, noise, offset-voltage, PSRR, CMRR and ICMR of amplifier are improved. The characteristics of LNA are successfully verified by the TSMC 0.35um 2P4M CMOS technology. There have a great potential in the VLSI implementation used in the portable electronic and bio-medicine product applications.

INTRODUCTION

Recently, the low noise amplifier (LNA) is a one of important device in the analog circuit which is used in communication, high-frequency, and the required high-precision circuit applications. The various structure of amplifier is desired for difference propose in the dedicate applications. The amplifiers have gained preponderance over other linear amplifier for low power and low-voltage applications. Based on the gain and band-width of amplifier is a trade–off. The amplifier has a high-gain and high bandwidth performance is an important design issue. The other consideration is appropriately designed exhibit much higher power efficiency over a wide modulation index range with rail-to-rail signal swing [1 - 5]. The transconductance operational amplifier has constant-gm to increase the stability, but its band-width much poor [1, 2]. The class-AB amplifier with complementary differential input stage adopted offset cancellation to improve the offset voltage problem for the LCD driver [3 - 5]. The Op-Amps has been compensated in Split-Length approach to process the frequency response compensation [6 - 9].

The common gate (CG) LNA uses double gm enhancement to provide input matching under low-power consumption. Feed-forward noise cancellation is employed in the LNA to suppress the noise from the CG transistor [9].

Digital TV receiver should be capable of handling signals with broadband frequency that it is required that a wideband LNA should have sufficiently high gain and low noise figure (NF) to obtain the high sensitivity. When the operation frequency increases, common source (CS) configuration suffers from low-power (LP) gain that the multi-cascade stage is required. The cascode topology is adopted to overcome the large chip size for LNA design. It makes a compromise between the noise figure (NF) and the chip size. All reported techniques can reduce the NF, but they still require a high supply voltage in the multicascode topology. Circuit analysis and simulations validate the advantages of

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proposed topology to encounter design specifications [11 - 14]. The organization of this paper is as follows. In first part, the compensation approaches for amplifier is presented. The structure of input stage with constant-g_m is shown in the second part. The third part, the hardware structure of LNA in CMOS circuit's realization is described. The simulations results are demonstrated and verified by HSPICE are shown in the fourth part. Finally, the conclusion is given.

CHANNEL-LENGTH SPLIT METHOD

The low-frequency noise is dominated from flick noise, is shown in the Fig. (**1**). Noise voltage v_n can be expressed by spectrum density in the equation (1) show that the second item is called flick noise can be effectively decreased by properly increasing the (W, L) geometry size of a transistor [10].

$$v_n^2 = \frac{i_n^2}{g_m^2} = \underbrace{\frac{8kT(1+\eta)}{3g_m}}_{\text{Thermal noise}}\Delta f + \underbrace{\frac{K_f}{2fC_{ox}WLK'}}_{1/f \text{ noise}}\Delta f \tag{1}$$
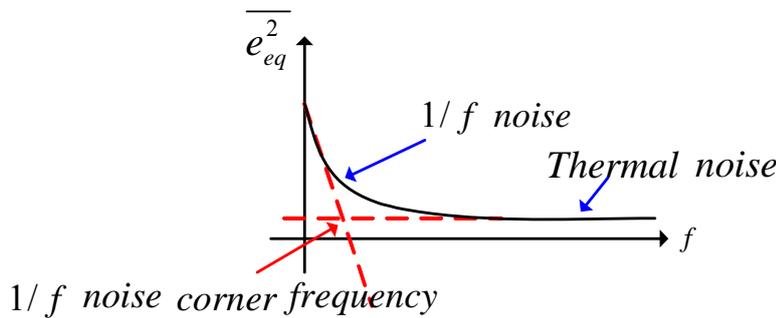

Fig. (1). Frequency spectrum for MOS noise voltage.

The totally capacitance is consist of inter-terminal, junction, line, and load capacitors for a MOS transistor at output node, that is $C_{tot} = C_{gd} + C_{db} + C_{line} + C_{load}$. The transistor is adopted larger width to improve the noise and also make the frequency response become to poor. Using channel length split technique to reduce the gate-channel capacitance to reach the band-width improved.
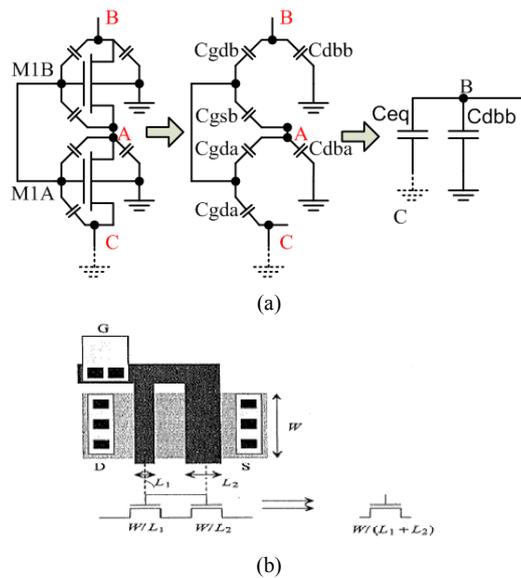

(a)

(b)

Fig. (2). Channel-length split (**a**) Equivalent model (**b**) Layout model.

The channel-length split method is separated differential input transistor into 2 transistors in series, is shown in Fig. (**2**). The area of M1B transistor is designed to large then M1A to decrease the effect of flicks noise and increase the value of *gm*. In the really design, the transistor connected to output terminal is used the larger width. The equivalent

circuits show that node A is floating-point and node C is virtual-ground. The equivalent capacitance C_{eq} from output node B is defined the serial path for C_{gdb} to C_{gsa} and C_{gdb} to C_{dba}. The equivalent capacitance changes to small base on the smaller capacitor C_{gsa} or C_{dba} in serial with the path. The channel-length split technique is reduced the total capacitance to improve the frequency response and take high gain. The split node is provided to use the indirect-compensation [6 - 9]. The channel-split used in PMOS and NMOS differential pairs are split to two transistors in serial that the node E and F to form low-impedance point is shown in Fig. (**6**). The output terminal feedback to those nodes is compensated by the miller capacitor. The amplifier applied the channel-split and the indirect compensation has the higher gain-bandwidth multiplication at low-noise.

INPUT-STAGE AND OUTPUT-STAGE

A. Input-Stage with Constant-gm

Base on take the good performance for input common mode range (ICMR) and wide-swing ability in the input stage of operational amplifier. The md1/md4 and md5/md8 are two set of PMOS and NMOS differential pair to improve the range of ICMR and wide-swing. The md2/md3 and md6/md7 are used to control the clamping circuit to limit the current of differential pair. Integrated both circuit to make a constant-g_m circuit is shown in Fig. (**3**). The operating mode of constant-g_m circuit is respectively described for three regions as below.
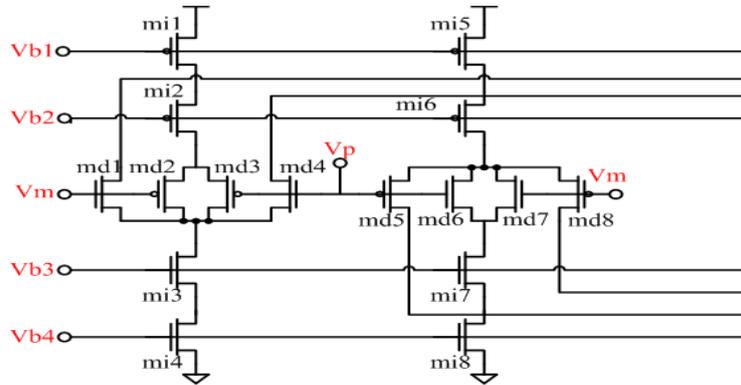

Fig. (3). Constant-gm circuit.

Region I: when $V_{CM, I} V_{DD}-2V_{SDP,SAT} -V_{SGP}$, the differential pair (PMOS) is turn on and the other differential pair (NMOS) is lie in triode or turn-off region. Because g_m^2 is proportion to current that let I_{i5} is equal to $4*I_{ref}$. Then the twice I_{ref} is flow-through md5/md8, respectively. The totally g_m expression is formulated during region I as (2).

Let $\beta_4 = \beta_5 = \beta$ and $I_{Dd4} = I_{Dd5} = I$

$$g_{mI} = g_{mP} = \sqrt{2\beta_5 2I_{Dd5}} = 2\sqrt{\beta_5 I_{Dd5}} = 2\sqrt{\beta I} \tag{2}$$

Where g_{mI} is express the transconductanc of differential pair for the region I.

Region II: When common mode voltage $V_{CM,II} > V_{SS} + 2V_{DSN,SAT} + V_{GSN}$ and $V_{CM,II} V_{DD} - 2V_{SDP,SAT} - V_{SGP}$. Because both PMOS and NMOS differential pair are turn on. Then the totally transconductance g_m is rising up that is $g_{mII} = g_{mN} + g_{mP}$. The clamping circuit md2/md3 and md6/md7 are used to limit its current. So that, the md1/md4 and md5/md8 flow-through current is limited at $Iref/2$ to induce the g_{mN} and g_{mP} are reduced. Its totally gm is expressed for region II as (3).

$$g_{mII} = g_{mN} + g_{mP}$$
$$= \sqrt{2\beta_4 \frac{I_{Dd5}}{2}} + \sqrt{2\beta_5 \frac{I_{Dd5}}{2}} = 2\sqrt{\beta I} \tag{3}$$

Region III: When $V_{CM,III} > V_{SS} + 2V_{DSN,SAT} + V_{GSN}$, the PMOS differential pair is lie in triode or turn-off region and the NMOS differential pair is turn on. The totally gm expression is formulated for region III as (4).

$$g_{mIII} = g_{mN} = \sqrt{2\beta_4 2I_{Dd4}} = 2\sqrt{\beta_4 I_{Dd4}} = 2\sqrt{\beta I} \tag{4}$$

The proposed differential pair can be provided a constant transconductance value during in the ranges for the operating region, where the values of g_{mI}, g_{mII} and g_{mIII} are equal to $2\sqrt{\beta I}$. We can show that the performance of the two sets input differential pairs in the amplifier has a rail-to-rail and constant-g_m for the input signal, is shown in the Fig. (**4**).
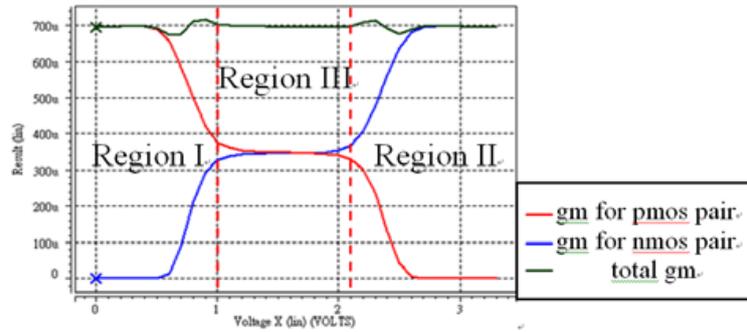

Fig. (4). Transconduction *vs*. input differential pair voltage.

B. Floating Class AB Output-Stage

The operation of the traditional output amplifier is like as inverter that the transfer characteristic curve is expressed by the red line in the Fig. (**5**). The result show that the curve has large slop related with the variation for the gate voltage of transistor to make the output swing can not reach rail-to-rail level. The proposed output stage is used the floating-potential structure in the class-AB amplifier to change the gate voltage of two transistors. The ratio of W/L in the transistor is properly tuning to adjust the variation of $V_{DS.}$ The transfer characteristic curve is expressedby the blue line in the Fig. (**5**). The simulation result show that the floating-potential and the properly ratio of W/L approaches can improve the amplifier to reach rail-to-rail output swing.
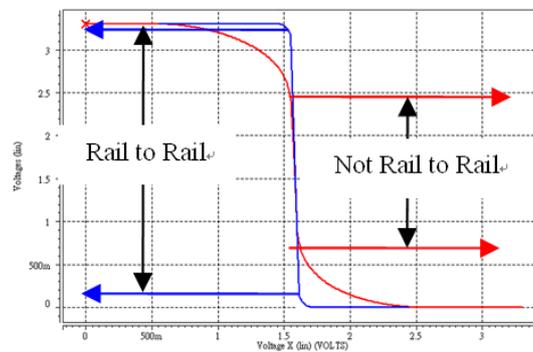

Fig. (5). Transfer characteristic curve.

LNA CMOS CIRCUIT REALIZATION

The folded-cascode operational amplifier with rail-to-rail, constant-gm input stage, and high-gain is shown in Fig. (**6**). The pre-stage is adopted folded-cascode circuit to produce full-swing and the output-stage is used class-AB push-pop amplifier. The amplifier used differential input structure with PMOS and NMOS in parallel be able to increase the range of ICMR value. The expression of the common mode voltage as (5) and (6)

$$V_{CM,MAX} = V_{DD} - 2V_{SGP,SAT} + V_{THN} \tag{5}$$

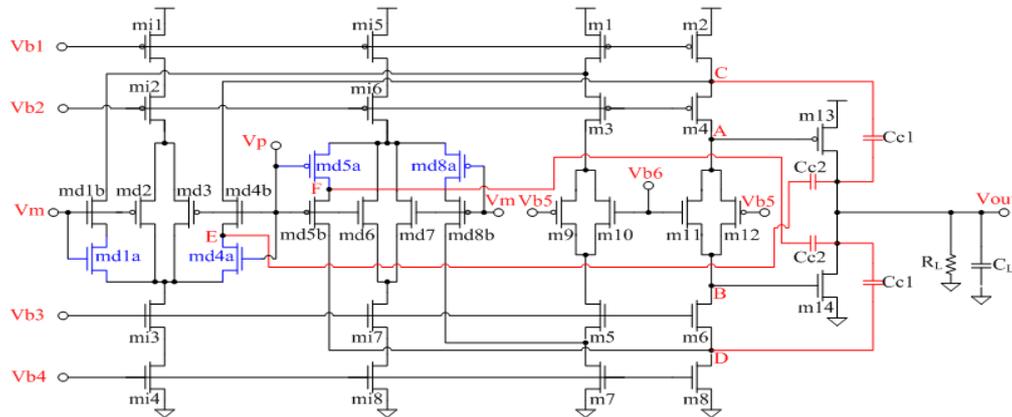$$V_{CM,MIN} = V_{SS} + 2V_{DSN,SAT} + V_{THP} \tag{6}$$

Fig. (6). The folded-cascode operational amplifier with capacitance cancellation.

The MOS transistor pair md1a/md1b, md4a/md4b, md5a/md5b, and md8a/md8b are the differential structure with channel length split, where md1a, md4a, md5a, and md8a are operated in triode region. The transistors mi1, mi2, md2, md3, mi7, mi8, md6, and md7 construct the current clamping circuit. The differential pairs for PMOS and NMOS are acted by the used clamping circuit to limit the current flow and to reduce the transconductance of transistors. The output stage consisted by transistors m11~m14 is a class-AB push-pull amplifier with transconductance amplification properties. When the gate-source voltage (V_{gs}) in the m8 is changed, then the V_{gs} of m14 also follow changed by the current mirror pair. That is, the amplifier can translate input voltage variation into the related output current. The output node A and B is floating points in the LNA produce a feature for the output impedance independent to load. The load current is determined by the W/L ratio at output stage m13 and m14, power supply, and loads, is shown in Fig. (**6**).
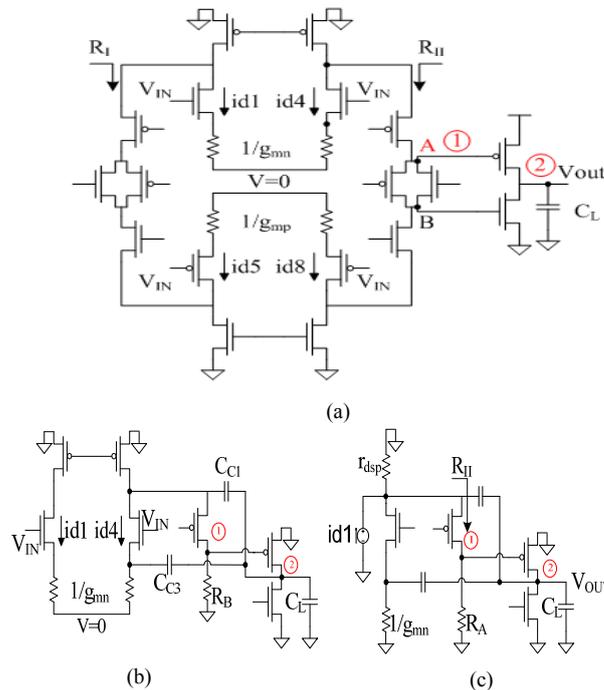

(a)

(b)   (c)

Fig. (7). (**a**) Small signal equivalent circuit for LNA. (**b**) Equivalent circuit for output of point A. (**c**) Equivalent circuit for (**b**).

The small signal equivalent circuit of the proposed LNA is shown in Fig. (**7a**). Assume point A is the output of 1-st stage. The concisely small signal equivalent circuits are shown in Fig. (**7b**, **c**). The small-signal analysis and the gain computing are based on the equivalent circuits.

$$R_{II} = \frac{r_{ds4} + g_{ds6}r_{ds6}(r_{ds8} \, // \, r_{dsd5})}{1 + g_{ds4}r_{ds4}} \tag{7}$$

$$i_{m7} = i_{m8} \approx -\frac{V_{IN}}{r_{md1a} + r_{md1b}} \tag{8}$$

$$i_{m4} = \frac{V_{IN}}{r_{md1a} + r_{md1b}}\frac{1}{(1+k)} \tag{9}$$

$$k = R_{II}\left(g_{ds2} + g_{dsd4}\right) \approx \frac{R_A\left(g_{ds2} + g_{dsd5}\right)}{g_{m4}r_{ds4}} \tag{10}$$

The output resistance R_A of the first stage is shown as below.

$$R_A = R_{ocasn} \, // \, R_{ocasp} \tag{11}$$
$$\approx g_{m4}\,r_{ds4}(r_{ds2} \, // \, r_{dsd4}) \, // \, g_{m6}r_{ds6}(r_{ds8} \, // \, r_{dsd5})$$

$$Av1 = \frac{2+k}{1+k}\frac{R_A}{r_{mIa} + r_{mIb}} \tag{12}$$

$$Av2 \approx \left(g_{m13} + g_{m14}\right)R_L \tag{13}$$

The small-signal model of the proposed LNA is shown in Fig. (**8**). The R_I ($R_{II)}$ and C_I (C_{II})are expressed the equivalent impedance and capacitance from A (V_{out}) terminal of output stage, respectively. Two sets compensation capacitors are connected to point C, D, E, and F as shown in Fig. (**6**). The buffer current i_{cc} through compensation capacitor and transistor from output of amplifier feedback to the output point at 1-st amplifier. The buffer current i_{cc} is expressed in (14):
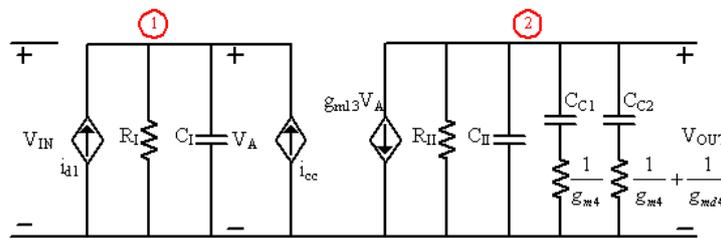

Fig. (8). Small signal model.

$$i_{CC} = i_{cc1} + i_{cc2} = \frac{Vout}{\dfrac{1}{sC_{C1}} + \dfrac{1}{g_{m4}}} + \frac{Vout}{\dfrac{1}{sC_{C2}} + \dfrac{1}{g_{m4}} + \dfrac{1}{g_{md4}}} \tag{14}$$

From the small signal model can find the transfer function is expressed as $V_{out}(s)/V_{in}(s) = N(s)/D(s)$, where N(s) and D(S) are shown in as:

$$N(s) = g_{mI} g_{mII} R_I R_{II} \left(1 + \frac{sC_{C1}}{g_{m4}}\right)$$

$$\bullet \left(1 + \frac{g_{m4} g_{md4} SC_{C2}}{g_{m4} + g_{md4}}\right) \tag{15}$$

$$D(s) = 1 + S[R_I C_I + R_{II} C_{II} + g_{mII} R_I R_{II}$$
$$(C_{C1} + C_{C2})] + S^2 (R_I R_{II} C_I C_{II}$$
$$+ \frac{g_{m4} + 2g_{md4}}{g_{m4} g_{md4}} g_{mII} R_I R_{II} C_I C_{II})$$

Let N(S) of transfer function equal to zero then the zero Z_1 and Z_2 of the system are solved as:

$$Z_1 = -\frac{g_{m4}}{C_{C1}} \quad and \quad Z_2 = -\frac{g_{m4} + g_{md4}}{g_{m4} g_{md4} C_{C2}} \tag{16}$$

Let D(S) of transfer function equal to zero then the pole P_1 and P_2 of the system are solved as:

$$P_1 = -\frac{1}{g_{mII} R_I R_{II} (C_{C1} + C_{C2})}$$

$$P_2 = -\frac{g_{mII}(C_{C1} + C_{C2})}{C_I C_{II} + \dfrac{g_{m4} + 2g_{md4}}{g_{m4} g_{md4}} g_{mII}(C_{C1} C_{C2})} \tag{17}$$

To calculate the band-width of LNA at unit gain is:

$$f_{unit} = \frac{g_{m13} + g_{m14}}{2\pi(C_{C1} + C_{C2})} \tag{18}$$

SIMULATION RESULTS

To verify the validity of the proposed LNA, the amplifier is simulated by HSPICE for CMOS technology. We can show that the folded cascade amplifier have rail-to-rail and constant-gm properties for the input signal. As the simulation results, the open loop gain of amplifier is 98.8dB, band-width is 60MHz, and phase margin (PM) is 60° at 30pf load capacitance, are shown in Fig. (**9**). Noise and slew-rate analysis are shown in Fig. (**10, 11**), respectively. The performances for the different compensation methods are simulated are expressed in Table **1**. Miller capacitor compensation is from output connect to points A and B. Miller with zero resistance compensation is from output connect to points A and B. Indirect compensation SL1 is from output connect to points A and B. Indirect compensation with channel separate SL2 is from output connects to points C, D, E, and F. The SL2 has a wide band-width and settle-time better than others. Detail the simulated data for the proposed LNA with SL2 compensation is summary in the Table **2**. The performance of the proposed LNA is more batter than the published papers for the same CMOS technology.
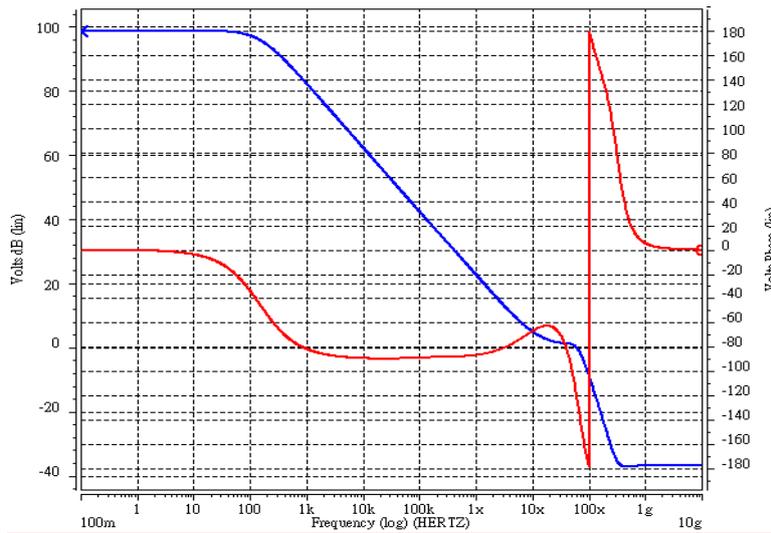
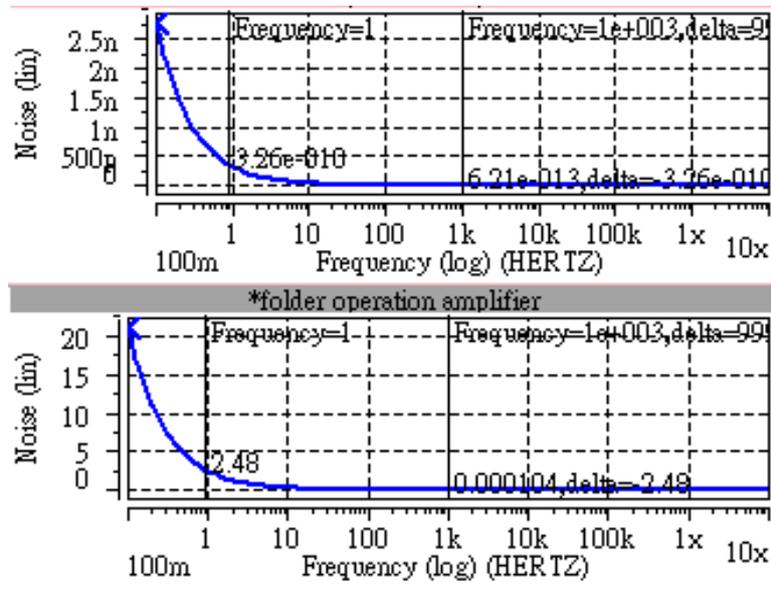**Fig. (9).** Frequency response of LNA (BW=60MHz, PM=60°).

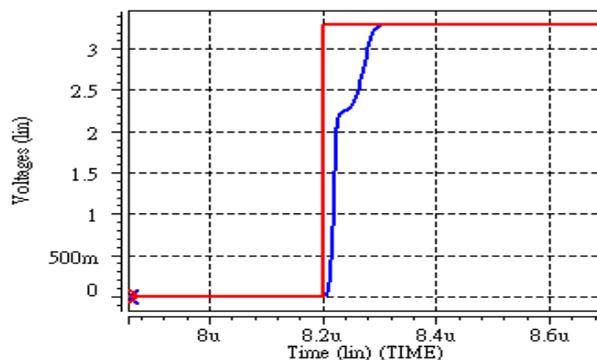**Fig. (10).** Simulation for LNA noise.

Fig. (11). Simulation for LNA slew-rate.

Table 1. Performance for various compensation techniques @CL=30pf.

	ADC dB	PM	fun MHz	Ts μs	Cc1 pf	Cc2 (Rz)
Miller	98.8	60	12.68	0.44	1.3	
miller with Rz	98.8	60	43.7	0.44	1.5	7.6k Ohm
SL1	98.8	60	35.9	0.134	0.6	
SL2	98.8	60	60	0.1	0.4	1.5

Table 2. Performance summary.

	This work	**Lu's [4] amplifier**	**Weng's [4] amplifier**	**Hong's[5] amplifier**
Process technology	0.35μm CMOS	0.35μm CMOS	0.35μm CMOS	0.35μm CMOS
VDD	3.3	5V	3.3V	5V
Input/Output range	0~3.3V	0~5V	0.05~3.25V	0~5V
Noise @ 1kHz	24.92n $V/\sqrt{Hz}$	NA	NA	NA
DC gain	98 dB	82 dB	65 dB	NA
Unity-gain frequency	60MHz	3.6MHz	750 kHz	NA
Phase margin	60°	80°	50°	>45°
Slew rate	154 V/μs	NA	NA	NA
Offset voltage	25.78μV	0.48mV	NA	6.1mV
Active area	252x235 m^2	103x40 m^2	86x73.5 m^2	100x100 m^2

LNA is fabricated using the different MOS topologies that act as an amplifier along with the biasing circuitry. Therefore, the behaviors function of the proposed LNA is successfully verified by the TSMC 0.35μm 2P4M CMOS technology. The required die size for the desired chip is 1268μm×1176μm after layout, is shown in the Fig. (**12**). The power dissipation is estimated about 2.8mW.
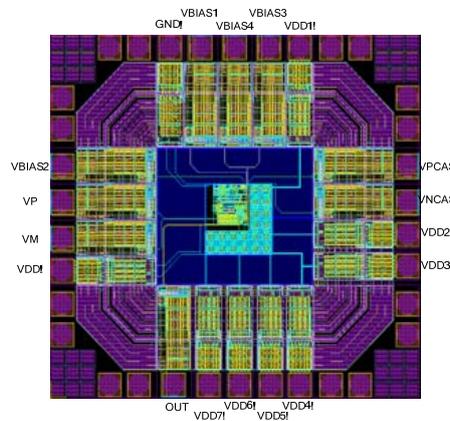

Fig. (12). Chip layout.

CONCLUSION

The folded-cascade operational amplifier with rail-to-rail is realized in CMOS circuits, and verified by HSPICE for TSMC technology. The channel-length split approach applied to 2 PMOS and NMOS pairs into the differential pair of the proposed LNA can be obtained constant-gm in input stag, low-noise (24.92n) and low offset-voltage (25.78μV) properties. The amplifier with floating-potential and the properly ratio of W/L approaches to improve the rail-to-rail output swing. The double indirect-frequency compensation technique and the clamping circuit are adopted to increase the bandwidth. The proposed circuit has a high band-width (BW=60MHz), DC gain (98dB) and constant-gm for high stability, good sensitivity and distortion. The power supply rejection ratio (PSRR, 114.8 dB) and CMRR (137.8 dB) and input common mode range (ICMR) has been improved. The proposed LNA is successfully implemented by the TSMC

0.35μm 2P4M silicon CMOS technology. The required die size for the desired chip is a 1268μm×1176μm layout area.

CONFLICT OF INTEREST

The authors confirm that this article content has no conflict of interest.

ACKNOWLEDGEMENTS

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